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Characterization and Compensation of High Speed Digitizers

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Abstract –
Increasingly, ADC technology is being pressed into service for single-shot instrumentation applications that were formerly served by vacuum-tube based oscilloscopes and streak cameras. ADC technology, while convenient, suffers significant performance impairments. Thus, in these demanding applications, a quantitative and accurate representation of these impairments is critical to an understanding of measurement accuracy. We have developed a phase-plane behavioral model, implemented it in SIMULINK and applied it to interleaved, high-speed ADCs (up to 4 gigasamples/sec). We have also developed and demonstrated techniques to effectively compensate for these impairments based upon the model.

Keywords – *high speed digitizer, characterization, modeling, compensation, phase plane, time-interleaved ADC*

I. INTRODUCTION

A number of technologies including streak cameras, vacuum tube based oscilloscopes, and high bandwidth digitizers based on analog digital converters (ADCs) are commonly used to record high-speed single-shot signals. ADC technology-based digitizers are becoming more prominent due to widespread commercial availability and support. This paper investigates the behavior of these digitizers for demanding single-shot measurements in support of scientific and national security missions, techniques for quantitative predictions of the impact ADC impairments will have on these single-transient measurements, and some techniques for impairment compensation. We have captured the essentials of ADC performance in a behavioral model. The model can be used to simulate the behavior of the ADC on arbitrary signals including those that are difficult to create on the bench-top. This predictive simulation capability is of interest for the prediction of instrumentation fidelity on complex, large scale, and expensive single-shot science experiments.

Commercial high-speed digitizers are typically composed of front-end analog circuitry to condition, scale and offset the input signal and a number of ADCs whose samples are interleaved to form the output [1]. Since the internal design of the digitizer and its components are often not known to its end users, it is desirable that a model rely on as little prior knowledge about the inner workings as possible. Modeling ADC behavior as a function of input state and slope has been explored many times [2,3]. These models, known as phase plane models, are based only on measurements of the ADC and can be extended to model digitizers composed of multiple ADCs.

Phase plane models have also been used to compensate for errors introduced by the analog digital conversion process [2,3,4]. These techniques result in significant improvements in signal to noise ratio and spurious free dynamic range.

There has also been significant work on modeling and compensating time interleaved ADC systems. A theoretical model to analyze the behavior of time interleaved systems is explored in [1]. Compensation methods are discussed in [5] and [6]. Reference [6] focuses on hardware based correction of timing errors while [5] works with relatively low frequency signals in simulation.

We have combined some of the features of these previous modeling efforts and extended their application to higher frequencies and interleaved ADCs. Compensation techniques based on our model are also explored.

II. THE ADC MODEL

In an ideal ADC, a continuous input signal is transformed into discrete output values at equally spaced time intervals, t_i. The discrete values are the result of quantization into bins with evenly spaced transitions, *T[k]* [7]. In real world ADCs, a noisy signal is quantized at varying time intervals into unevenly spaced bins.

In time-interleaved ADC systems, additional error is introduced by mismatches and timing errors between the individual ADCs [1,5,6]. Each ADC will have slightly different transition levels, gain, and offset.

Figure 1 illustrates our modeling approach. Gaussian noise is added to the signal before it is sampled at discrete times and quantized by an interleaved set of transition levels.

A set of tables of slope dependent transition levels defines the quantizer bins. In this table the column index is identified with a slope and the row index is identified with a code bin. The values of the table elements correspond to the ADC threshold values for a specified slope and code bin value. It is not practical to measure the threshold value at each combination of slope and code bin value, so the model linearly interpolates in the slope axis to generate the necessary threshold matrix density in phase-space. One table is needed to describe each ADC in the system. The table also implicitly encodes the gain and offset.

Fig. 1. ADC Model realized in Mathworks Simulink simulation software

A number of techniques to measure the elements of the table exist. The histogram method given by [7] can be applied to a series of sine wave measurements [2]. This technique only covers ellipses in the phase plane. More recently, techniques using two tones to more effectively cover the phase plane have been developed [3]; a technique for optimizing the choice of the two frequencies has also been developed [8]. Our model is independent of the technique used to obtain the transition table.

The amplitude noise and jitter parameters can also be determined from data records. The amplitude noise level determines the noise floor of the system. It can be set by trial and error until the simulated noise floor matches the measured noise floor. Reference [7] also specifies methods to measure both amplitude noise and jitter.

III. SIMULATION RESULTS

The model was tested using sine wave records from an Acqiris DC271 4 GS/s digitizer. It achieves 4 GS/s by interleaving 4 ADCs at 1 GS/s. The sine waves were generated by an Agilent E8247C low noise signal generator, and a K&L Microwave tunable bandpass filter was used to remove any harmonics.

Nonlinearities in the transition levels cause harmonic distortion [9]. Gain mismatch errors in the ADCs cause distortion at the interleave frequency plus and minus the fundamental signal frequency, while offset mismatches appear at the interleave frequency [5].

The model parameters were derived from a dataset consisting of records of sine waves at 7.9 dBm, 10.9 dBm, 13.9 dBm, 16.9 dBm, and 19.9 dBm. The frequencies were chosen according to the IEEE 1057 near 30 MHz, 60 MHz, 125 MHz, 250 MHz, and 400 MHz. Figure 2 shows the frequency spectrum of both a recorded 16.9 dBm signal and simulated signal. The recorded signal was not part of the dataset used to set the model parameters. The two signals are plotted offset from each other for clarity. The simulated

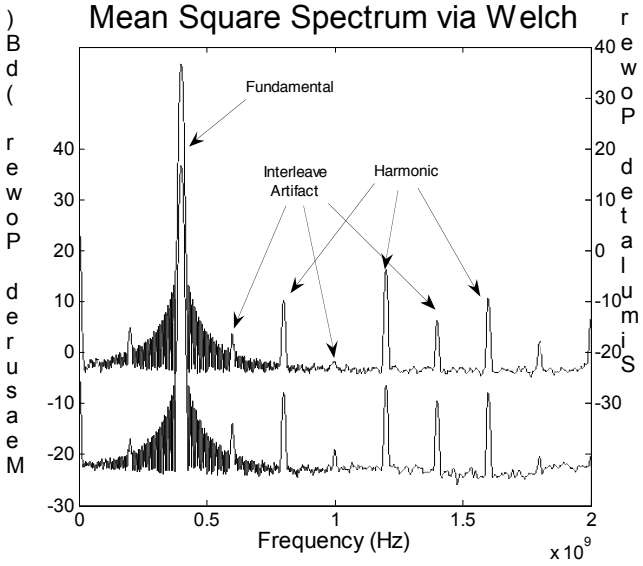

Fig. 2. Frequency spectrum of measured (bottom) and simulated (top) signals

signal exhibits both the harmonic distortion and interleave artifacts.

Testing the model in simulation against recorded data shows that it correctly models the impairments introduced by real digitizers.

IV. SAMPLE RATE DEPENDENCE OF LINEARITY AND EFFECTIVE NUMBER OF BITS (ENOB)

Data collected from an Acqiris DC271 digitizer and shows that the ENOB of measurements vary with sample rate and number of ADCs interleaved. The mean absolute value of differential nonlinearity (DNL) and effective number of bits were compared for data records taken at various sample rates and number of ADCs per channel. Figure 3 shows the DNL plotted versus sample rate for the Acqiris digitizer. The DNL

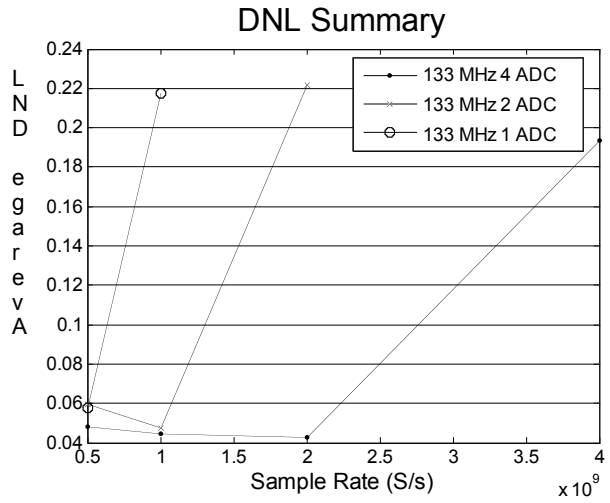

Fig. 3. DNL vs sample rate

improves as the sample rate of the individual ADCs decreases.

Figure 4 shows the ENOB plotted versus sample rate. The ENOB improves as sample rate decreases, but fewer ADCs at a higher sample rate produce a better ENOB than more ADCs are lower sample rates. This suggests that the interleaving effects are outweighing the gain in linearity.

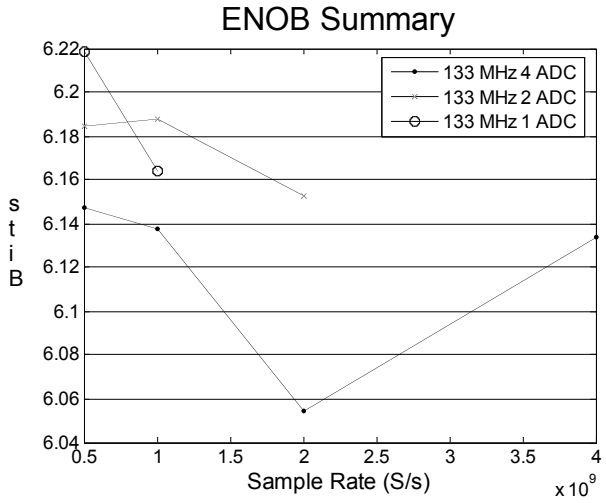

Fig. 4. ENOB vs sample rate

V. COMPENSATION TECHNIQUES

The measurement impairments in our model can be divided into two groups, those that describe random effects (amplitude noise, jitter) and those that describe "fixed-pattern" effects (gain, offset, transition levels). Fixed-pattern effects can be compensated for while the random effects cannot. We discuss compensation only for these fixed-pattern impairments.

A. Transition Level (TL) Compensation

In transition level compensation, each code k is replaced by the mid point between its transition levels [2,3,10]. As in the model, the transition levels are interpolated along the slope dimension.

$$x[t] = k$$
$$\hat{x}[t] = \frac{T[k,s] + T[k+1,s]}{2} \quad (1)$$

However, since the slope of the input signal is unknown a system of two equations must be solved. For a given k, $T[k,s]$ is piece wise linear in s. The slope at sample t can be estimated with a finite difference, $s = \frac{\hat{x}[t] - \hat{x}[t-\Delta t]}{\Delta t}$.

B. Independent Transition Level (ITL) Compensation

A straightforward extension of TL compensation is to extract the transition level table for each interleaved ADC separately and use the appropriate transition level table for each sample. This also implicitly compensates for gain and offset mismatches.

C. Interleave (Int) Compensation

Given the offset, gain, and time errors of the interleaved ADC system, the original signal can be reconstructed by subtracting the offsets, dividing by the normalized gains, and interpolating in the time direction [5]. In many high speed / high bandwidth signal recording applications, the signal frequency will not be significantly smaller than the Nyquist frequency. In such cases, linear interpolation performs similarly to higher order methods [6].

These parameters can be estimated by performing a four parameter sine wave fit to the whole data record obtaining the parameters A, θ, C, and ω [7]. The data record is then divided into pieces corresponding to each ADC. For each piece, a three parameter fit is performed fixing ω, yielding A_i, θ_i, and C_i. The relative gain of the ADCs is $\frac{A_i}{A}$. The relative offsets are C-C_i. The time offset is given by $\frac{\theta_i - \theta}{\omega}$. Care must be taken when subtracting because the θ values are wrapped to be between $-\pi$ and π.

D. Transition Level and Interleave (ITL) Compensation

Interleave compensation alone will not correct for harmonic distortion caused by transition level nonlinearities. Interleave compensation can be applied after TL compensation to remove both types of distortion.

Experimental results indicate that there is no significant gain from applying Int compensation after ITL compensation.

VI. COMPENSATION RESULTS

Table 1 shows the results of applying the compensation techniques to 233 MHz data collected on an Acqiris DC271. Figure 5 shows the resulting spectra. The parameters used in the compensation methods were derived from a dataset consisting of sine wave records at frequencies of 400,250,200, and 125 MHz; at amplitudes of 19.9, 16.9, 13.9,10.9,7.9 dBm for each frequency (at total of 20 distinct sine wave records).

Table 1. Compensation Results

Technique	ENOB (averaged over sampling frequency)
Raw data	6.139
TL	6.247
ITL	6.261
Int	6.165
Int + TL	6.276

ITL and TL + Int show similar results and perform the best. Int compensation gives a relatively small increase in ENOB because the energy in the interleave artifacts is much smaller than the energy in the harmonics.

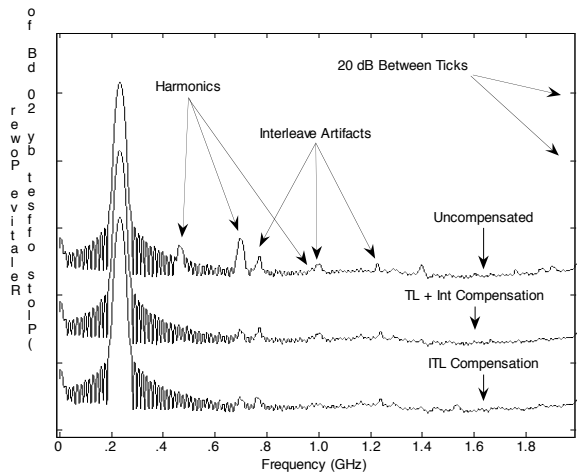

Fig. 5. Effect of compensation on power spectra

Figure 6 shows the result of applying Int compensation and TL+int compensation on data taken at various sample rates and with varying numbers of ADCs on an Acqiris DC271. The performance of TL+int decreases as the sample rate decreases due to the slope estimation becoming poorer. With Int compensation the ENOB becomes roughly constant and independent of the number of ADCs or sample rate.

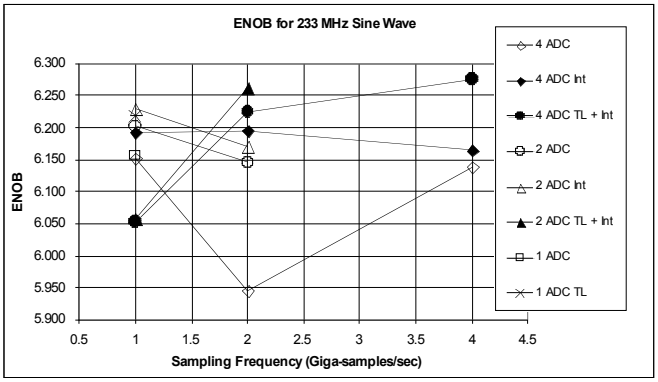

Fig. 6. ENOB for measured and compensated data

VII. CONCLUSIONS AND FUTURE WORK

Our digitizer model accurately models the measurement impairments found in real world digitizers. In addition, compensation techniques based on this model are able to improve ENOB. Interleaving ADCs reduce the ENOB because of impairments introduced by the interleaving process. By compensating for these effects, the ENOB is effectively independent of the number of ADCs interleaved together. Furthermore, compensation for transition level effects gives additional gains.

In the future, we will examine the model performance on larger data sets and other ADCs. In addition, we will compare the model's simulation results to measurements of single-impulse waveforms. It will also be interesting to investigate why ITL compensation gives similar results to Int + TL compensation. ITL compensation does not compensate for any timing errors.

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